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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2024**

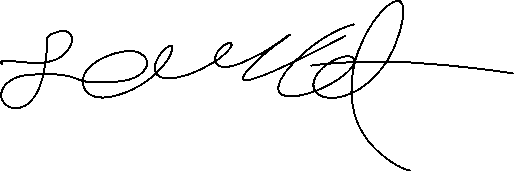
**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Logan Current**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Date: 09/26/2024**



**Report due date: 10/02/2024**

1. **OBJECTIVE**

The Objective of this lab is to learn how to layout an inverter and a NAND gate with three inputs using Cadence Virtuoso. As well as draw a stick diagram for each.

1. **PROCEDURE**

First, I drew a stick diagram for each to decide how I would start to make the layout. Then, calculated and made sure I understood the lambda rules for the layouts. After, I designed the inverter first in Cadence, checked it to make sure there were no errors in schematic then did the same thing for the NAND 3 gate.

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1. **RESULT**

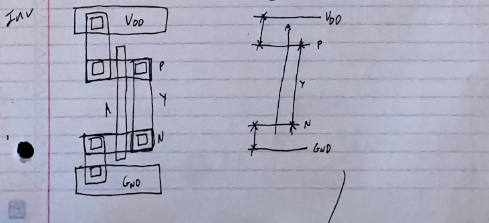
A computer screen shot of a computer screen

Description automatically generatedA computer screen shot of a computer program

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***A paper with drawings and numbers

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1. **CONCLUSION**

The Results from the layout were as expected. There were no errors with my design when I ran a DRC check on both gates. The hardest part was getting down and remembering the lambda rules for everything, had to double check my work many times to ensure I was following standard.